

Amendments to the Claims

1-31. (canceled)

32. (previously presented) A method of making a varactor comprising:

forming a plurality of alternating P- wells and N+ regions in a silicon layer of an SOI structure, wherein the P- wells form N+/P- junctions with the N+ regions, and wherein each of the P- wells and the N+ regions extends completely through the silicon layer to an insulation layer of the SOI structure;

forming a plurality of gate oxides, wherein each of the gate oxides is formed above a corresponding one of the P- wells;

forming a plurality of silicon gates, wherein each of the silicon gates is formed above a corresponding one of the gate oxides;

electrically coupling each of the silicon gates together; and,

electrically coupling each of the N+ regions together.

33. (previously presented) The method of claim 32 wherein each of the silicon gates comprises a polysilicon gate.

34. (previously presented) The method of claim 32 wherein the SOI structure includes a layer of high resistivity silicon under the insulation layer over.

35. (previously presented) The method of claim 32 where in the insulation layer comprises sapphire.

36. (previously presented) The method of claim 32 where in the insulation layer comprises an oxide.

37. (previously presented) The method of claim 32 wherein the P- wells form a transistor body, and wherein the transistor body is allowed to float.

38. (previously presented) The method of claim 32 wherein each of the silicon gates is formed so as to have a width to length ratio of approximately 16 to 1.

39. (previously presented) The method of claim 32 wherein the varactor has a capacitive switching ratio equal to or greater than 5.

40. (previously presented) The method of claim 32 wherein the varactor has a capacitive switching ratio equal to or greater than 20.